MTR05\_

Digital Systems

Unit 2 Combinational Systems

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**Team members:**

Name: Registration:

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**DIGITAL SYSTEMS**

**UNIT 2 COMBINATIONAL SYSTEMS**

**Learning result:** The student will be able to carry out simulations using specialized software and physically implement combinational systems for the automation of industrial proceses using digital logic systems.

**Theoretical framework:**

Investigate the following topics:

* Combinational logic circuits:
* Propagation delay:
* Bit, Nibble, Byte:
* MSB & LSB:
* “Don’t care” values:
* Gray code:
* Sum of products (SOP):
* Boolean Algebra:
* Karnaugh Maps:
* Integration scales of integrated circuits: SSI, MSI, LSI, VLSI, ULSI:
* Voltage ranges for the logic levels of TTL digital ICs:
* Multiplexer (MUX):
* Arithmetic logic unit (ALU):

**Laboratory equipment:**

* 1 Altera DE2 FPGA development board with the FPGA Cyclone II EP2C35F672C6

**Development:**

a) Install the software: Quartus II web edition and Multisim.

b) Design the following combinational systems using schematic diagrams in Multisim, make the corresponding VHDL code and simulate each system in the Quartus II software indicated in the practice folders, finally physically implement each system in the Altera DE2 development board.

*NOTE: In each of the cells, place what is requested, in the codes place text (not an image of the text), in the simulations place an impression of the cropped screen.*

**1) AND:** Do a system that verify the truth table of the AND gate.

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| **Schematic/Simulation in Multisim** |
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| **Behavioural VHDL code** |
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| **Structural VHDL code** |
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| **Quartus II Simulation** |
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**2) OR:** Do a system that verify the truth table of the OR gate.

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| **Schematic/Simulation in Multisim** |
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| **Behavioural VHDL code** |
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| **Structural VHDL code** |
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| **Quartus II Simulation** |
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**3) NOT:** Do a system that verify the truth table of the NOT gate.

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| **Schematic/Simulation in Multisim** |
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| **Behavioural VHDL code** |
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| **Structural VHDL code** |
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| **Quartus II Simulation** |
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**4) NAND:** Do a system that verify the truth table of the NAND gate.

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| **Schematic/Simulation in Multisim** |
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| **Behavioural VHDL code** |
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| **Structural VHDL code** |
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| **Quartus II Simulation** |
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**5) NOR:** Do a system that verify the truth table of the NOR gate.

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| **Schematic/Simulation in Multisim** |
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| **Behavioural VHDL code** |
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| **Structural VHDL code** |
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| **Quartus II Simulation** |
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**6) XOR:** Do a system that verify the truth table of the XOR gate.

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| **Schematic/Simulation in Multisim** |
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| **Behavioural VHDL code** |
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| **Structural VHDL code** |
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| **Quartus II Simulation** |
|  |

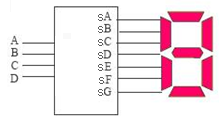
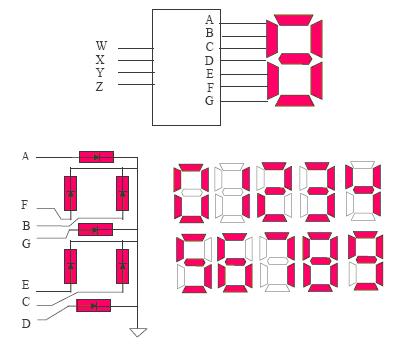
**7) XNOR:** Do a system that verify the truth table of the XNOR gate.

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| **Schematic/Simulation in Multisim** |
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| **Behavioural VHDL code** |
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| **Structural VHDL code** |
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| **Quartus II Simulation** |
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**8) BINGRAY:** Do a system that verify the 4 bits BINARY to GRAY converter.

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| **Schematic/Simulation in Multisim** |
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| **Behavioural VHDL code** |
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| **Structural VHDL code** |
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| **Quartus II Simulation** |
|  |

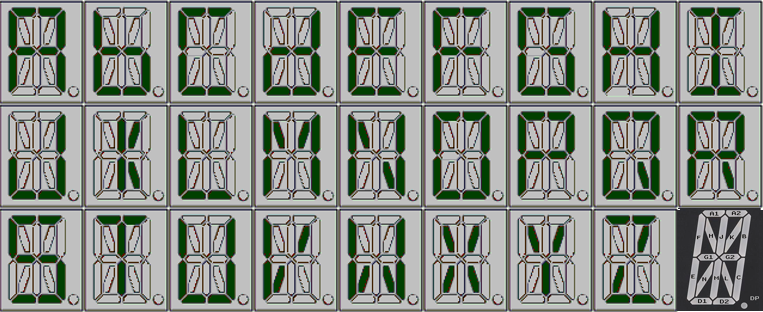
**9) D7SEG:** Complete the table placing the equations for decoding from 4-bit binary to decimal (0 to 9 only) on a common cathode 7-segment display.

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| **A** | **B** | **C** | **D** |  | **sA** | **sB** | **sC** | **sD** | **sE** | **sF** | **sG** |
| 0 | 0 | 0 | 0 |  |  |  |  |  |  |  |  |
| 0 | 0 | 0 | 1 |  |  |  |  |  |  |  |  |
| 0 | 0 | 1 | 0 |  |  |  |  |  |  |  |  |
| 0 | 0 | 1 | 1 |  |  |  |  |  |  |  |  |
| 0 | 1 | 0 | 0 |  |  |  |  |  |  |  |  |
| 0 | 1 | 0 | 1 |  |  |  |  |  |  |  |  |
| 0 | 1 | 1 | 0 |  |  |  |  |  |  |  |  |
| 0 | 1 | 1 | 1 |  |  |  |  |  |  |  |  |
| 1 | 0 | 0 | 0 |  |  |  |  |  |  |  |  |
| 1 | 0 | 0 | 1 |  |  |  |  |  |  |  |  |
| 1 | 0 | 1 | 0 |  |  |  |  |  |  |  |  |
| 1 | 0 | 1 | 1 |  |  |  |  |  |  |  |  |
| 1 | 1 | 0 | 0 |  |  |  |  |  |  |  |  |
| 1 | 1 | 0 | 1 |  |  |  |  |  |  |  |  |
| 1 | 1 | 1 | 0 |  |  |  |  |  |  |  |  |
| 1 | 1 | 1 | 1 |  |  |  |  |  |  |  |  |

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| **Schematic/Simulation in Multisim** |
|  |
| **Behavioural VHDL code** |
|  |
| **Structural VHDL code** |
|  |
| **Quartus II Simulation** |
|  |

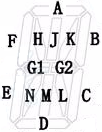
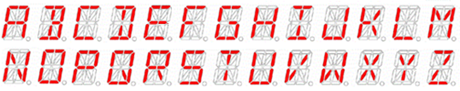
**10. D16SEG:** Design a common anode 16-segment alphanumeric display decoder that shows the text: “MECHATRONICSENGINEERING”. Complete the chart including the missing values, as well as the text of the structural VHDL code and images of the simulation with all possible cases.



|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | **A** | **B** | **C** | **D** | **E** | **sA1** | **sA2** | **sB** | **sC** | **sD1** | **sD2** | **sE** | **sF** | **sG1** | **sG2** | **sH** | **sJ** | **sK** | **sL** | **sM** | **sN** | **Hexa** |
| **0** | M | 0 | 0 | 0 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **1** | E | 0 | 0 | 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **2** | C | 0 | 0 | 0 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **3** | H | 0 | 0 | 0 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **4** | A | 0 | 0 | 1 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **5** | T | 0 | 0 | 1 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **6** | R | 0 | 0 | 1 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **7** | O | 0 | 0 | 1 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **8** | N | 0 | 1 | 0 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **9** | I | 0 | 1 | 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **10** | C | 0 | 1 | 0 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **11** | S | 0 | 1 | 0 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **12** | E | 0 | 1 | 1 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **13** | N | 0 | 1 | 1 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **14** | G | 0 | 1 | 1 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **15** | I | 0 | 1 | 1 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **16** | N | 1 | 0 | 0 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **17** | E | 1 | 0 | 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **18** | E | 1 | 0 | 0 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **19** | R | 1 | 0 | 0 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **20** | I | 1 | 0 | 1 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **21** | N | 1 | 0 | 1 | 0 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **22** | G | 1 | 0 | 1 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **23** |  | 1 | 0 | 1 | 1 | 1 | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **XXXX** |
| **24** |  | 1 | 1 | 0 | 0 | 0 | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **XXXX** |
| **25** |  | 1 | 1 | 0 | 0 | 1 | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **XXXX** |
| **26** |  | 1 | 1 | 0 | 1 | 0 | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **XXXX** |
| **27** |  | 1 | 1 | 0 | 1 | 1 | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **XXXX** |
| **28** |  | 1 | 1 | 1 | 0 | 0 | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **XXXX** |
| **29** |  | 1 | 1 | 1 | 0 | 1 | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **XXXX** |
| **30** |  | 1 | 1 | 1 | 1 | 0 | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **XXXX** |
| **31** |  | 1 | 1 | 1 | 1 | 1 | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **XXXX** |

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| **VHDL Code** |
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| **Quartus II Simulation** |
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**11. D16SEGv2:** Design a common anode 16-segment alphanumeric display decoder that shows the text from A to Z. Complete the chart including the missing values, as well as the text of the structural VHDL code and images of the simulation with all possible cases.

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|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **TABLE** | | **AA** | **BB** | **CC** | **DD** | **EE** | **A** | **B** | **C** | **D** | **E** | **F** | **G1** | **G2** | **H** | **J** | **K** | **L** | **M** | **N** | **Hexa** |
| **0** | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | **043F** |
| **1** | B | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | **03AD** |
| **2** | C | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | **18FF** |
| **3** | D | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | **03ED** |
| **4** | E | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | **183F** |
| **5** | F | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | **1C7F** |
| **6** | G | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | **10BF** |
| **7** | H | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | **243F** |
| **8** | I | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | **1BED** |
| **9** | J | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | **21FF** |
| **10** | K | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | **3C73** |
| **11** | L | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | **38FF** |
| **12** | M | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | **24D7** |
| **13** | N | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | **24DB** |
| **14** | O | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | **00FF** |
| **15** | P | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | **0C3F** |
| **16** | Q | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | **00FB** |
| **17** | R | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | **0C3B** |
| **18** | S | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | **123F** |
| **19** | T | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | **1FED** |
| **20** | U | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | **20FF** |
| **21** | V | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | **3CF6** |
| **22** | W | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | **24FA** |
| **23** | X | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | **3FD2** |
| **24** | Y | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | **3FD5** |
| **25** | Z | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | **1BF6** |
| **26** |  | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | **X** |
| **27** |  | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | **X** |
| **28** |  | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | **X** |
| **29** |  | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | **X** |
| **30** |  | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | **X** |
| **31** |  | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | **X** |

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| **VHDL Code** |
|  |
| **Quartus II Simulation** |
|  |

**Individual conclusions**

**Name:**

**Name:**

**Name:**

**Name:**

**U2 Practice report (50%)**

|  |  |  |  |
| --- | --- | --- | --- |
| **Value** | **Reactive** | **Y** | **N** |
| 10% | Before the deadline, only a file per team in word format is sent to the email guillermo.guerrero@upa.edu.mx without eliminating this checklist, in the name of the file put the letter of the group, first name and first surname of one of the team members. The cover includes the letter of the group in the corresponding place, full names and UP of the team members. It includes the name and individual conclusion of at least one paragraph of four lines per student, it doesn’t have any misspelling. |  |  |
| 5% | Includes each of the topics of the theoretical framework. |  |  |
| 5% | Completes the cells of practice 1, physically delivers it to the professor. |  |  |
| 5% | Completes the cells of practice 2, physically delivers it to the professor. |  |  |
| 5% | Completes the cells of practice 3, physically delivers it to the professor. |  |  |
| 5% | Completes the cells of practice 4, physically delivers it to the professor. |  |  |
| 5% | Completes the cells of practice 5, physically delivers it to the professor. |  |  |
| 5% | Completes the cells of practice 6, physically delivers it to the professor. |  |  |
| 5% | Completes the cells of practice 7, physically delivers it to the professor. |  |  |
| 10% | Completes the cells of practice 8, physically delivers it to the professor. |  |  |
| 10% | Completes the cells of practice 9, physically delivers it to the professor. |  |  |
| 15% | Completes the cells of practice 10, physically delivers it to the professor. |  |  |
| 15% | Completes the cells of practice 11, physically delivers it to the professor. |  |  |
| **Qualification:** | | | |